REMARKS

The application has been reviewed in light of the Office Action dated June 22, 2004. Claims 1-39 were pending in this application, with claims 1, 9, 17, 25, 29, 33 and 37-39 being in independent form. By this Amendment, new claim 40 has been added. It is submitted that no new matter has been introduced. Support for the new claim can be found in the application at, for example, page 10, line 17 through page 12, line 6.

Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,481,469 to Brasen et al. in view of U.S. Patent No. 5,625,803 to McNelly et al. Claims 1-39 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over U.S. Patent No. 5,535,370 to Raman et al. in view of U.S. Patent No. 5,521,834 to Crafts et al. and further in view of U.S. Patent No. 5,493,508 to Dangelo et al.

Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claims 1, 9, 17, 25, 29, 33 and 37-39 are patentable over the cited art, for at least the following reasons.

The present application relates to estimation of electric power consumption by integrated circuits which are comprised of basic cells and mega cells. More specifically, the application is directed to tools for estimating electric power consumption by an integrated circuit which use information collected during logic simulation.

Applicants found that power consumption of an integrated circuit can be more accurately estimated by estimating electric power consumed by mega cells of the integrated circuit based on the logic simulations and pre-established power consumption data, in addition to estimating electric power consumed by basic cells of the integrated circuit. The application describes techniques for estimating electric power consumed by the mega cells which include estimating a

current consumed by the mega cells by simulating logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells. For example, the alternating current component of the current consumed by the mega cells for each logic state is determined by utilizing a predetermined constant value and the average operation frequency for the logic state. The techniques of this application generate more accurate estimations of power consumption of integrated circuits than conventional techniques.

Brasen, as understood by Applicants, is directed to automatic generation of input vectors for power simulation. According to one embodiment of Brasen (FIG. 7 and 8), simulation of power vectors for a plurality of blocks of logical elements in an integrated circuit is performed. In addition, a block BLOCK2 shown in FIGS. 7 and 8 of Brasen is a mega-cell which has "fixed power requirements" (for example, a ROM, RAM, etc.), in contrast to the blocks of combinatorial logic gates (for example, BLOCK1 and BLOCK3).

Since the mega-cell of Brasen has fixed power requirements, no logic simulation is needed for estimation of power consumption by the mega-cell. Brasen simply does not disclose or suggest simulating logic of the mega-cell and estimating power consumed by the mega-cell based on logic simulation. For example, Applicants find no teaching or suggestion in Brasen of determining an alternating current component of power consumed by the mega-cell.

McNelly, as understood by Applicants, is directed to a method of simulating power usage, by utilizing a power model that characterizes a cell's power consumption behavior as a two-part, piecewise-linear function based on signal slew rates and output load. According to the Office

Action, McNelly discloses calculating an alternating current component of power dissipation of logic elements.

However, Applicants do not find teaching or suggestion in McNelly of simulating logic of a mega-cell and estimating power consumed by the mega-cell based on logic simulation, as described by the claims of this application. For example, Applicants find no teaching or suggestion in McNelly of determining an alternating current component of power consumed by the mega-cell.

Therefore, even a combination of Brasen and McNelly fails to disclose each and every element of the claimed invention.

Raman, as understood by Applicants, is directed to calculating current and power consumption of a circuit prior to silicon, by utilizing simulation and test vectors along with a model of the circuit to estimate the current and power consumption of the circuit, as close to actual silicon results as possible. A characterization table of average current values is generated for different cell types and device types and different values of capacitive loads. An actual toggle count is determined for each node in the circuit during simulation. An activity factor can then be generated based on the toggle count during a sample time period and the number of clock cycles during the sample period. Using the activity period, the current is determined from the average current value for the device times the activity factor.

As acknowledged in the Office Action, Raman does not mention mega-cells and does not disclose or suggest any techniques of calculating the alternating current component of power consumed by mega-cells.

Crafts and Dangelo do not cure the deficiencies of Raman.

Crafts, as understood by Applicants, is directed to approximating dynamic power dissipation in a CMOS circuit attributed to charging of capacitive loads (within the circuit as well as external loads. According to Crafts, a determination is made of the capacitive load for each cell in a netlist for the CMOS circuit, from cell library data sheets. In addition, the capacitive loads of the interconnects between stages are estimated. A switching rate for each cell is then calculated, and the output frequency for the cell is determined. The power dissipation for each cell is calculated by multiplying the output frequency by the capacitive load. The dynamic power dissipation for the circuit is determined by summing the power dissipation terms for each of the cells in the netlist.

However, Crafts, like Raman, does not mention mega-cells and does not purport to disclose or suggest any techniques of calculating the alternating current component of power consumed by mega-cells.

Figure 2, items 30, 32 and 34, and column 4 line 1 through column 5, line 10 of Crafts discusses state transition analysis for the inputs of the circuit, and simply does not disclose or suggest that the discussion is relevant to calculating the alternating current component of power consumed by mega-cells.

Dangelo '508, as understood by Applicants, is directed to generating structural descriptions of complex digital devices from high-level descriptions and specifications. Dangelo '508 was cited in the Office Action as purportedly disclosing mega cells and hardware description languages.

However, Applicants do not find teaching or suggestion in the cited art of calculating the alternating current component of power consumed by mega-cells.

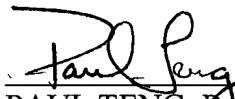
Accordingly, for at least the above-stated reasons, Applicant respectfully submits that

independent claims 1, 9, 17, 25, 29, 33 and 37-39, and the claims depending therefrom, are patentable over the cited art.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



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